C. Amendments to the Claims.

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- 1. (Currently Amended) An integrated circuit device, comprising:
  - a programmable portion comprising a plurality of circuits configurable by a user of the integrated circuit device; and

at least one communication portion comprising:

a plurality of data operation circuits, each of which performs a different function on received input data, including at least one circuit block manufactured to perform a predetermined data communication function including converting received first data values into second data values, the at least one circuit including a block converter circuit that converts an input data word into an output data word having different bit values than the input data word in response to a user selectable operational value, and

an operation control store that provides the user selectable operational value from a plurality of operational values to the at least one circuit to control the type of operation performed on the received data; and

a memory circuit for storing configuration information for configuring circuits of the programmable portion.

2. (Original) The integrated circuit device of claim 1, wherein:

the programmable portion comprises a programmable interconnect portion and a logic gate portion.

- 3. (Cancelled) The integrated circuit device of claim 2, further including:
  - a memory circuit for storing configuration information for configuring circuits of the programmable portion.
- 4. (Currently Amended) The integrated circuit device of claim 21, further including:

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a timing circuit that receives a clock signal and generates an internal clock signal that is phase shifted with respect to the clock signal.

# 5. (Original) The integrated circuit device of claim 1, further including:

a plurality of input/outputs commonly connected to programmable portion and the communication portion.

# 6. (Cancelled) The integrated circuit device of claim 1, wherein:

the communication portion includes a plurality of data operation circuits, each of which performs a different function on received input data.

#### 7. (Cancelled) The integrated circuit device of claim 6, wherein:

the data operation circuits include a block converter circuit that converts an input data word into an output data word having different bit values than the input data word.

### 8. (Currently Amended) The integrated circuit device of claim 61, wherein:

the data operation circuits include a scrambler circuit that performs a scramble operation on the received data represented by a scrambling polynomial.

#### 9. (Cancelled) The integrated circuit device of claim 6, wherein: 20

the communication portion further includes an operation control store that provides one of a plurality of operational values to the data operation circuits that controls the type of operation performed on the received data.

#### 10. (Currently Amended) The integrated circuit device of claim 91, wherein: 25

the data operation circuits include a scrambler circuit that performs a scramble operation on the received data; and

the operation control store provides operational values that represent at least one scrambling polynomial.

### 11. (Currently Amended) The integrated circuit device of claim 91, wherein:

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the operational control store includes circuits that may provides at least one user operational value configured by a user and preset operational values that are established by at least one integrated circuit manufacturing step.

#### 12. (Currently Amended) The integrated circuit device of claim 61, wherein:

the communication portion includes a data (MUX) multiplexer that enables a data path between one of a plurality of inputs and a data MUX output, and each data operation circuit is coupled to an input of the data MUX.

### 13. (Currently Amended) The integrated circuit device of claim 61, wherein:

the communication portion includes a physical layer circuit that provides a data output stream compatible with a particular data transmission media.

#### 14. (Currently Amended) The integrated circuit device of claim 61, wherein:

the at least one communication portion includes a plurality of communication portions.

# 20 15. (Currently Amended) A semiconductor device, comprising:

a programmable logic device having a communication portion embedded therein, the communication portion including nonprogrammable circuits designed to provide a selectable data communication function,

25 <u>the non-programmable circuits comprising a block converter</u> circuit that encodes input data words into output data words and a

scrambler circuit that scrambles data values according to a user selectable scrambling polynomial, and

an operational control store that provides the user selectable scrambling polynomial value to the scrambler circuit from a plurality of user selectable scrambling polynomial values.

16. (Original) The semiconductor device of claim 15, wherein:

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- the communication portion includes a plurality of circuit blocks that each provides a different data communication function.
- 17. (Original) The semiconductor device of claim 16, wherein:

the communication portion includes a selectable data path between 10 each circuit block and a data output.

18. (Cancelled) The semiconductor device of claim 15, wherein:

the communication portion includes a block converter circuit that encodes input data words into output data words and a scrambler circuit that scrambles data values according to an operational control value.

19. (Currently Amended) The semiconductor device of claim 15, wherein:

the communication portion includes a block converter circuit that decodes input data words into output data words and a de-scrambler circuit that de-scrambles data values according to an operational control value provided by the operational control store.

- 20. (Cancelled) The semiconductor device of claim 18, wherein:
- the communication portion includes an operational control store that provides selectable operational control values to the scrambler circuit. 25
  - 21. (Currently Amended) A method, comprising the steps of:

performing predetermined logic functions on a programmable logic portion of an integrated circuit; and

functions performing serial data communication communication portion of the integrated circuit that includes circuit blocks that are not synthesized with programmable logic device configuration data, the serial data communication functions being user selectable between

selecting a polynomial value from a number of user (i) selectable polynomial values, and

scrambling serial data according to the selected polynomial value, or

encoding serial data having words of a first bit length into (ii) serial data having words of a second bit length that is different than the first bit length.

### 22. (Cancelled) The method of claim 21, wherein:

performing serial data communication functions includes selecting a polynomial value from a number of polynomial values, and

scrambling serial data according to the selected polynomial value.

#### 23. (Cancelled) The method of claim 21, wherein: 20

performing serial data communication functions includes encoding serial data having words of a first bit length into serial data having words of a second bit length that is different than the first bit length.

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